

1-Mbit (64K x 16) Static RAM

Features

- **Very high speed**
 - 55 ns
- **Temperature Ranges**
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- **Wide voltage range**
 - 2.2V - 3.6V
- **Pin compatible with CY62126BV**
- **Ultra-low active power**
 - Typical active current: 0.85 mA @ f = 1 MHz
 - Typical active current: 5 mA @ f = f_{Max} (55 ns speed)
- **Ultra-low standby power**
- **Easy memory expansion with \overline{CE} and \overline{OE} features**
- **Automatic power-down when deselected**
- **Available in Pb-free and non Pb-free 48-ball VFBGA and 44-pin TSOP Type II packages**

Functional Description^[1]

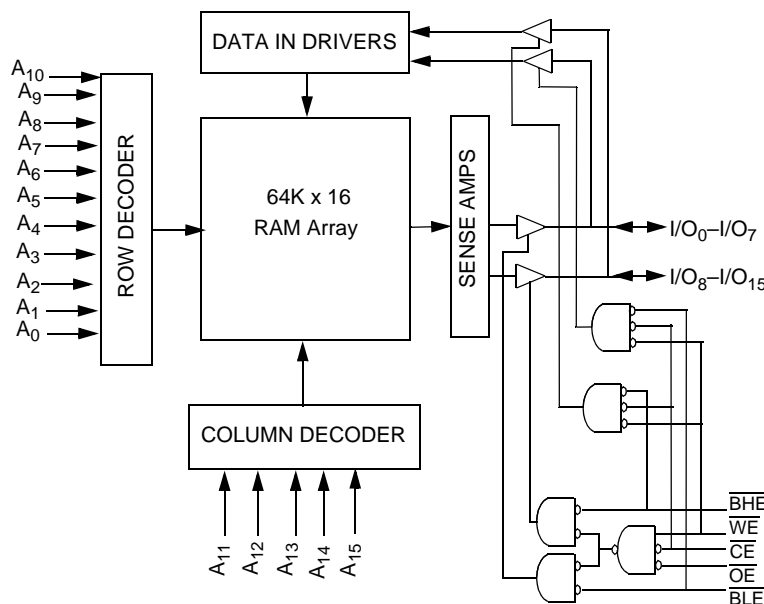
The CY62126DV30 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features

advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected (\overline{CE} HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , BLE HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram

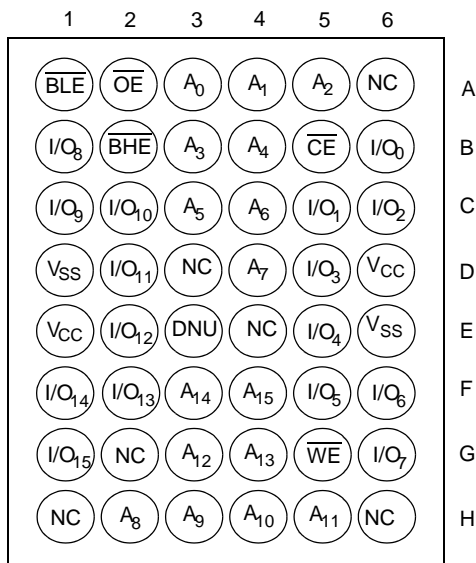
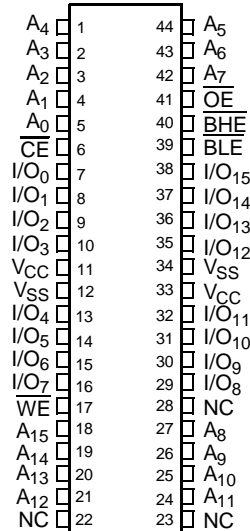


Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
		f = 1 MHz		f = f _{Max}							
		Min.	Typ.	Max.		Typ. ^[2]	Max.	Typ. ^[2]	Max.	Typ. ^[2]	Max.
CY62126DV30L	Automotive	2.2	3.0	3.6	55	0.85	1.5	5	10	1.5	15
CY62126DV30LL	Industrial				55	0.85	1.5	5	10	1.5	4

Pin Configurations^[3, 4]
**48-ball VFBGA
Top View**

**TSOP II (Forward)
Top View**

Notes:

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.
- NC pins are not connected to the die.
- E3 (DNU) can be left as NC or V_{SS} to ensure proper operation. (Expansion Pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M).

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential -0.3 to 3.9V
 DC Voltage Applied to Outputs in High-Z State^[6] -0.3V to V_{CC} + 0.3V

DC Input Voltage^[6] -0.3V to V_{CC} + 0.3V
 Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T _A)	V _{CC} ^[7]
Industrial	-40°C to +85°C	2.2V to 3.6V
Automotive	-40°C to +125°C	2.2V to 3.6V

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		CY62126DV30-55			Unit	
				Min.	Typ. ^[5]	Max.		
V _{OH}	Output HIGH Voltage	2.2V ≤ V _{CC} ≤ 2.7V	I _{OH} = -0.1 mA	2.0			V	
		2.7V ≤ V _{CC} ≤ 3.6V	I _{OH} = -1.0 mA	2.4				
V _{OL}	Output LOW Voltage	2.2V ≤ V _{CC} ≤ 2.7V	I _{OL} = 0.1 mA			0.4	V	
		2.7V ≤ V _{CC} ≤ 3.6V	I _{OL} = 2.1 mA			0.4		
V _{IH}	Input HIGH Voltage	2.2V ≤ V _{CC} ≤ 2.7V		1.8		V _{CC} + 0.3	V	
		2.7V ≤ V _{CC} ≤ 3.6V		2.2		V _{CC} + 0.3		
V _{IL}	Input LOW Voltage	2.2V ≤ V _{CC} ≤ 2.7V		-0.3		0.6	V	
		2.7V ≤ V _{CC} ≤ 3.6V		-0.3		0.8		
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		Ind'l	-1	+1	μA	
				Auto	-4	+4		
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		Ind'l	-1	+1	μA	
				Auto	-4	+4		
I _{CC}	V _{CC} Operating Supply Current	f = f _{Max} = 1/t _{RC}	V _{CC} = 3.6V, I _{OUT} = 0 mA, CMOS level		5	10	mA	
		f = 1 MHz			0.85	1.5		
I _{SB1}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V,$ $V_{IN} \leq 0.2V,$ $f = f_{Max}$ (Address and Data Only), $f = 0$ (\overline{OE} , \overline{WE} , \overline{BHE} and \overline{BLE})	L	Ind'l		1.5	5	μA
				Auto		1.5	15	
I _{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0, V_{CC} = 3.6V$	L	Ind'l		1.5	5	μA
				Auto		1.5	15	
			LL			1.5	4	

Notes:

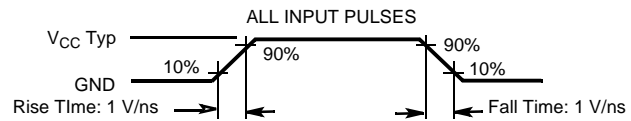
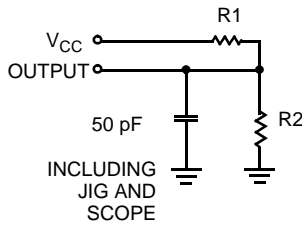
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.
- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns., V_{IH(max.)} = V_{CC} + 0.75V for pulse durations less than 20 ns.
- Full device operation requires linear ramp of V_{CC} from 0V to V_{CC(min)} & V_{CC} must be stable at V_{CC(min)} for 500 μs.

Capacitance^[8]

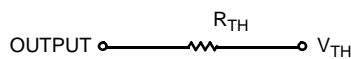
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	8	pF
C _{OUT}	Output Capacitance		8	pF

Thermal Resistance^[8]

Parameter	Description	Test Conditions	TSOP	VFBGA	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, 2-layer printed circuit board	55	76	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		12	11	°C/W

AC Test Loads and Waveforms


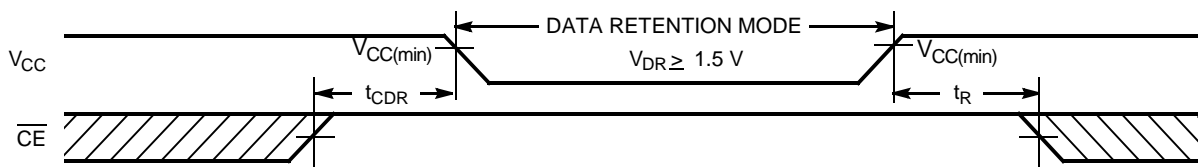
Equivalent to: THEVENIN EQUIVALENT



Parameters	2.5V	3.0V	Unit
R1	16600	1103	Ohms
R2	15400	1554	Ohms
R _{TH}	8000	645	Ohms
V _{TH}	1.2	1.75	Volts

Data Retention Characteristics

Parameter	Description	Conditions	Min.	Typ ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5			V
I _{CCDR}	Data Retention Current	V _{CC} =1.5V, $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V				μA
		L Ind'l			4	
		L Auto			10	
		LL Ind'l			3	
t _{CDR} ^[8]	Chip Deselect to Data Retention Time		0			ns
t _R ^[9]	Operation Recovery Time		100			μs

Data Retention Waveform

Notes:

8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} > 100 μs.

Switching Characteristics (Over the Operating Range)^[10]

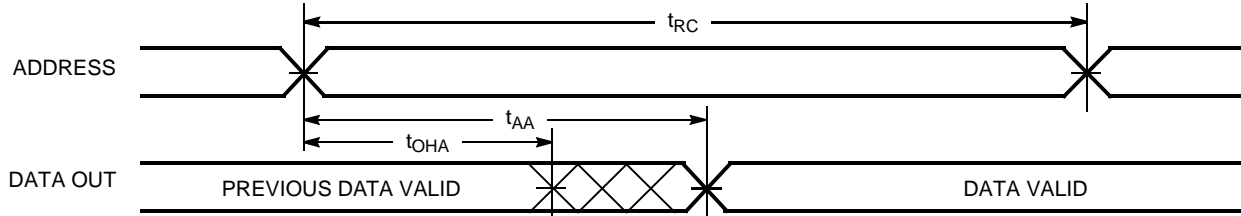
Parameter	Description	CY62126DV30-55		Unit
		Min.	Max.	
Read Cycle				
t _{RC}	Read Cycle Time	55		ns
t _{AA}	Address to Data Valid		55	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		55	ns
t _{DOE}	\overline{OE} LOW to Data Valid		25	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[11]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[11, 12]		20	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[11]	10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[11, 12]		20	ns
t _{PU}	\overline{CE} LOW to Power-up	0		ns
t _{PD}	\overline{CE} HIGH to Power-down		55	ns
t _{DBE}	$\overline{BLE/BHE}$ LOW to Data Valid		25	ns
t _{LZBE}	$\overline{BLE/BHE}$ LOW to Low Z ^[11]	5		ns
t _{HZBE}	$\overline{BLE/BHE}$ HIGH to High-Z ^[11, 12]		20	ns
Write Cycle^[13]				
t _{WC}	Write Cycle Time	55		ns
t _{SCE}	\overline{CE} LOW to Write End	40		ns
t _{AW}	Address Set-up to Write End	40		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	40		ns
t _{BW}	$\overline{BLE/BHE}$ LOW to Write End	40		ns
t _{SD}	Data Set-up to Write End	25		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[11, 12]		20	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[11]	10		ns

Notes:

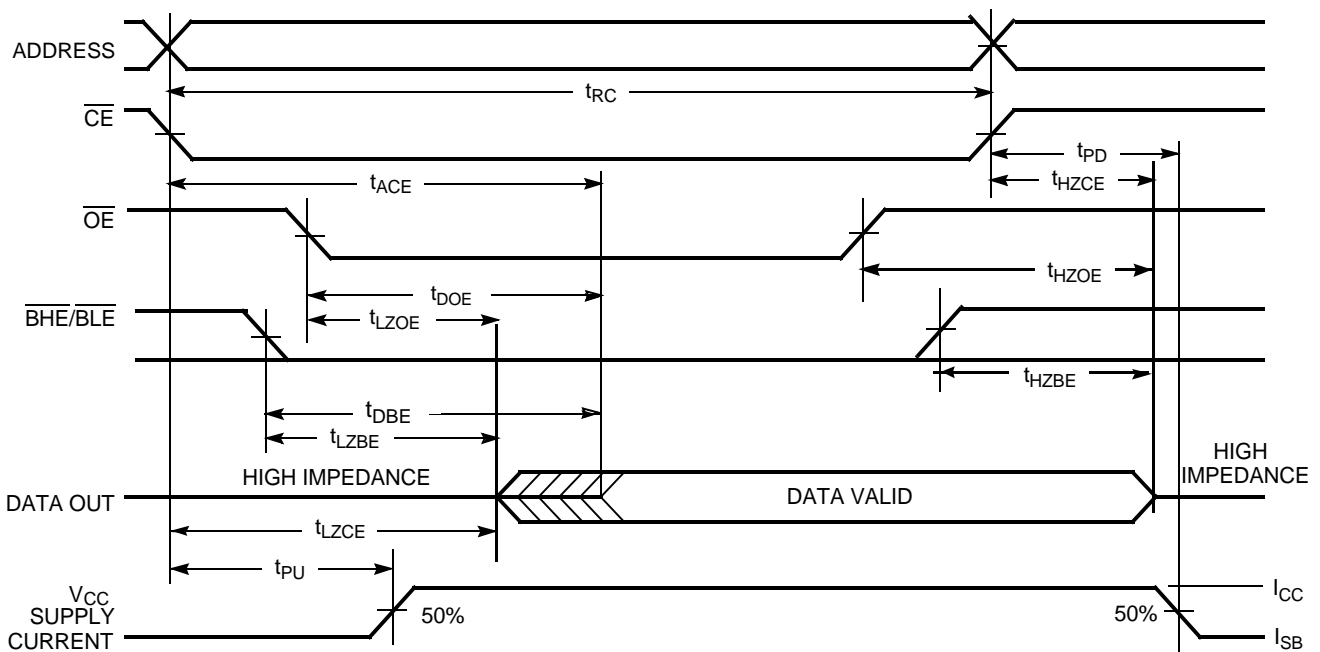
10. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL} .
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}.
12. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
13. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[14, 15]



Read Cycle No. 2 (\overline{OE} Controlled)^[15, 16]



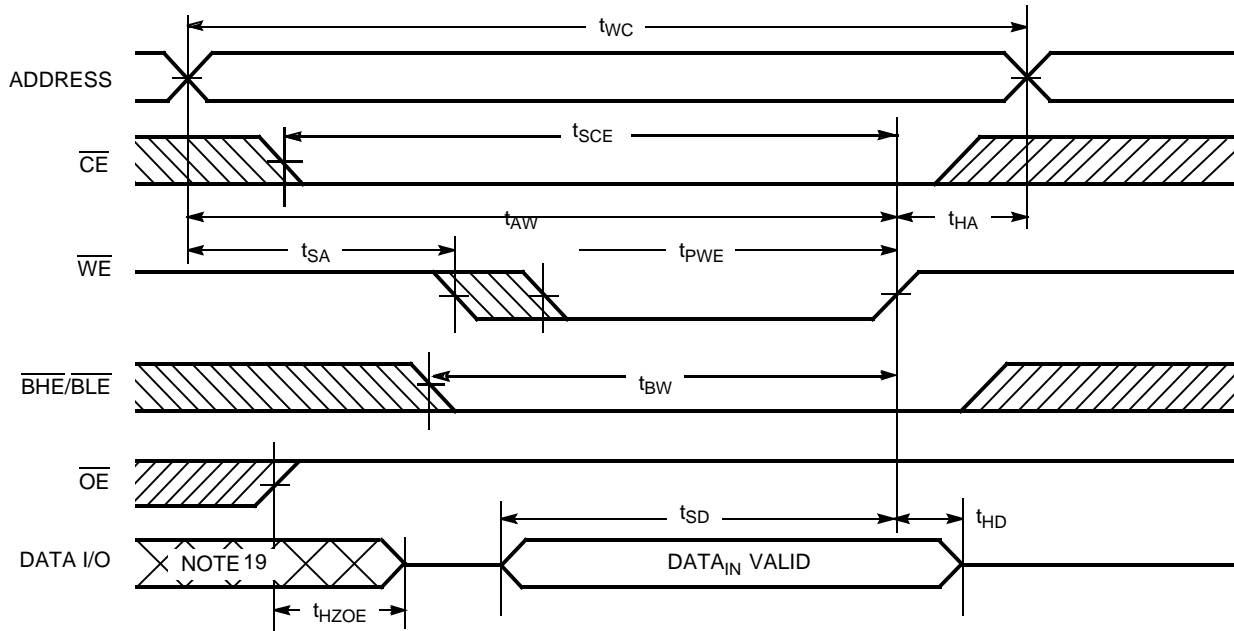
Notes:

- 14. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , $\overline{BLE} = V_{IL}$.
- 15. WE is HIGH for Read cycle.
- 16. Address valid prior to or coincident with \overline{CE} , \overline{BHE} , \overline{BLE} transition LOW.

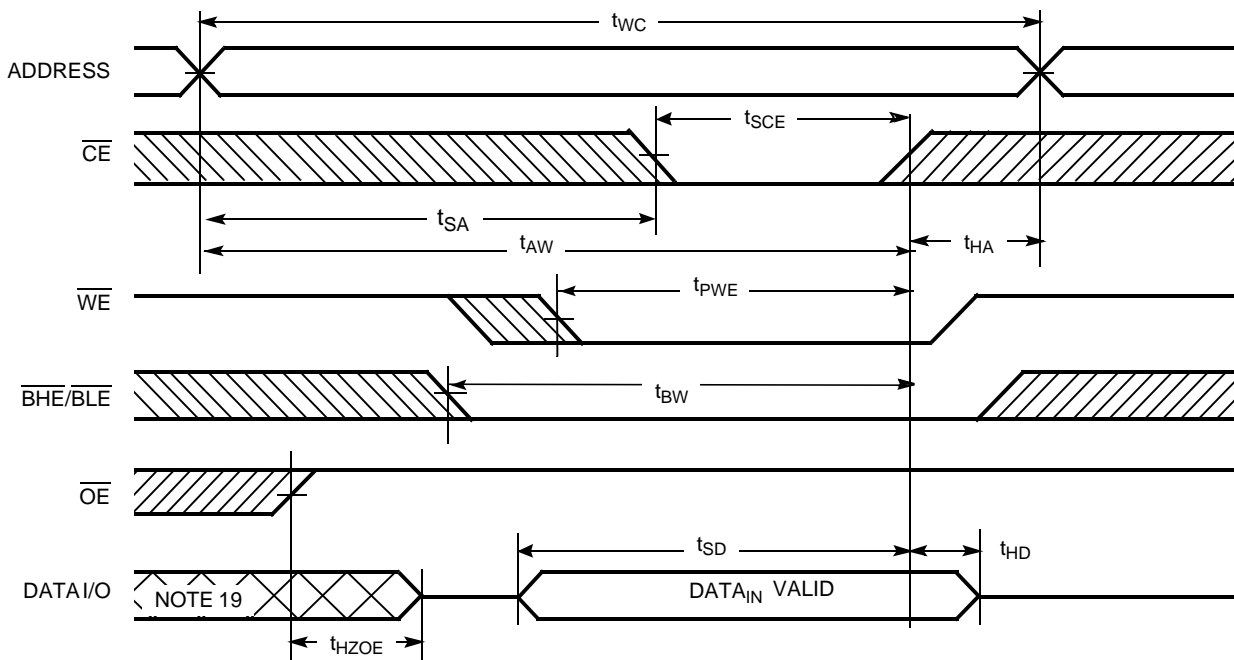
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Switching Waveforms(continued)

Write Cycle No. 1 (\overline{WE} Controlled)^[12, 13, 16, 17, 18]



Write Cycle No. 2 (\overline{CE} Controlled)^[12, 13, 16, 17, 18]



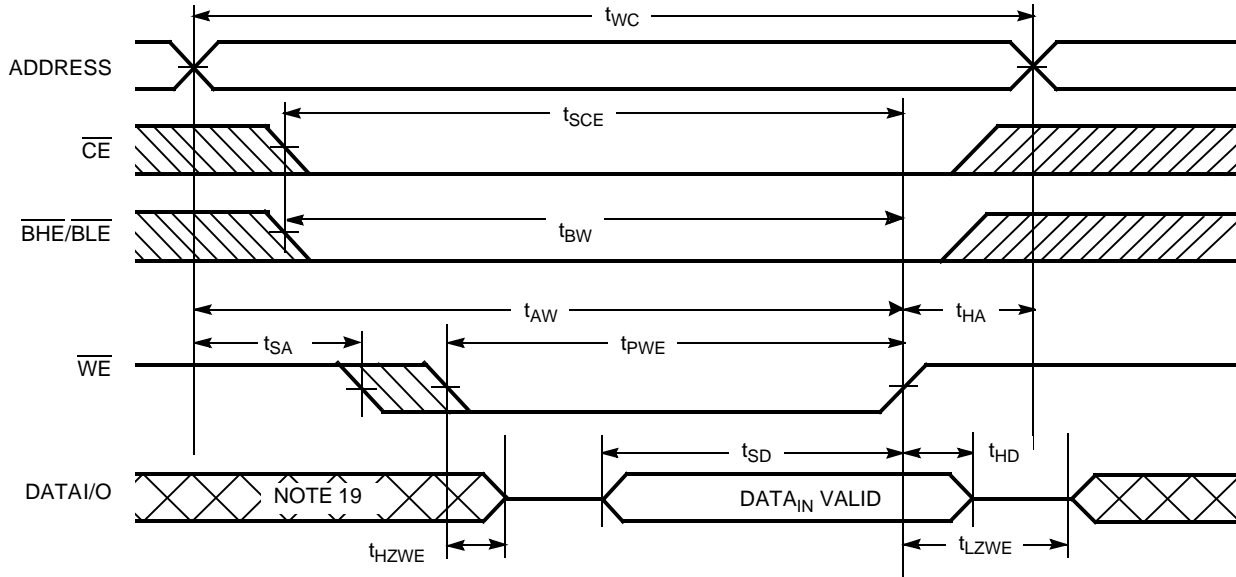
Notes:

- 17. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
- 18. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

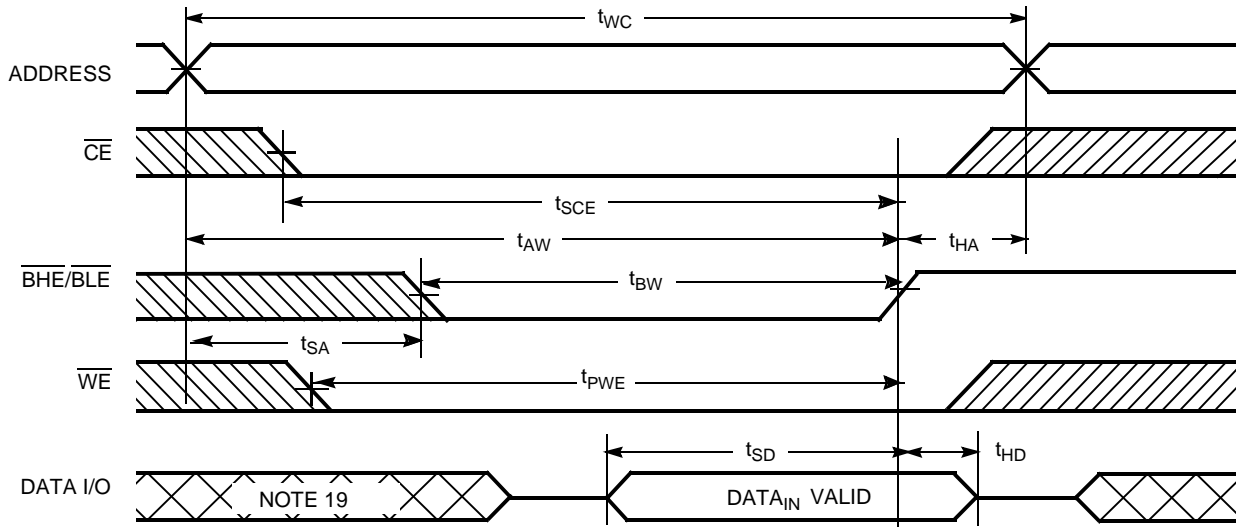
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Switching Waveforms(continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[17, 18]



Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ -controlled, \overline{OE} LOW)^[17, 18]



Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	High Z (I/O_8 – I/O_{15}); Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); High Z (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	High Z (I/O_8 – I/O_{15}); Data In (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8 – I/O_{15}); High Z (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})

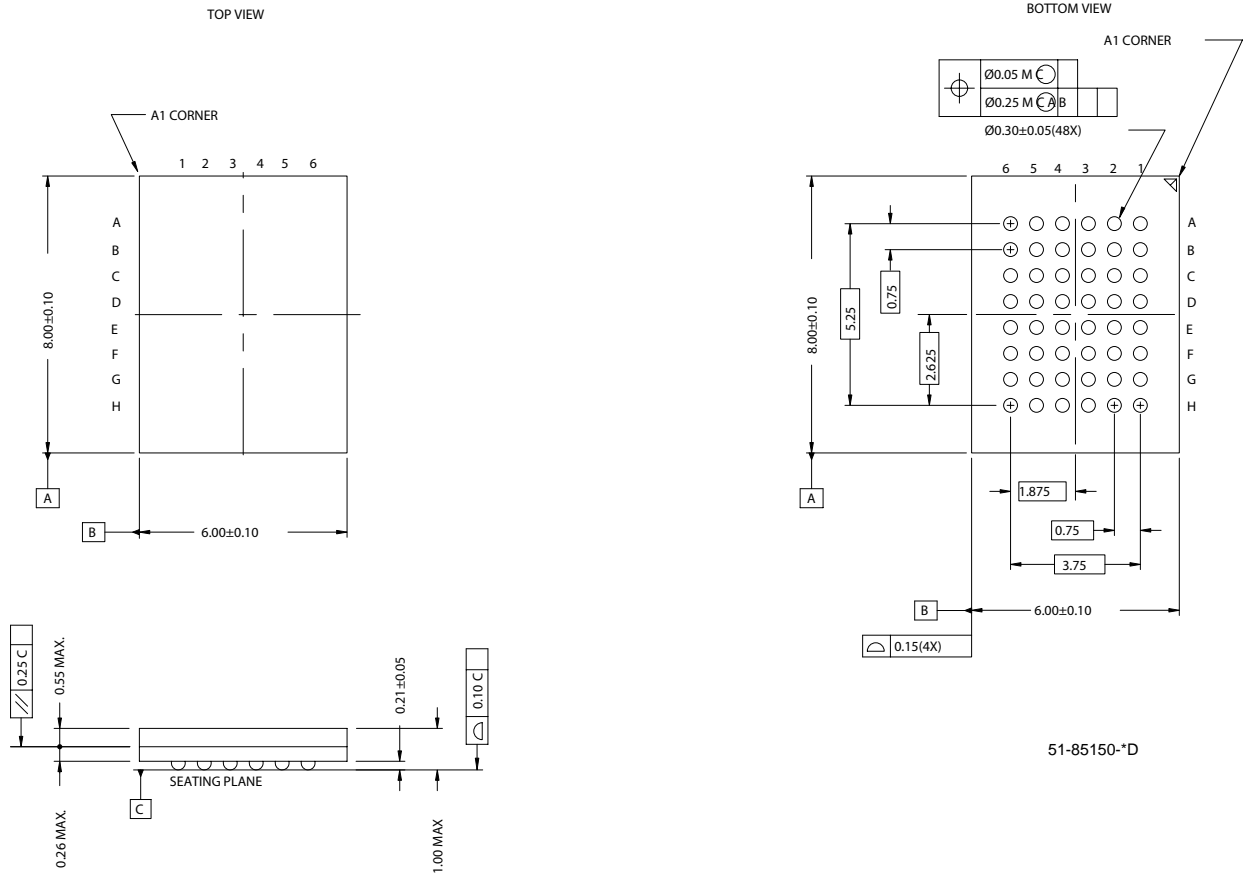
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62126DV30LL-55BVI	51-85150	48-ball Fine-Pitch Ball Grid Array (6 x 8 x 1 mm)	Industrial
	CY62126DV30LL-55BVXI		48-ball Fine-Pitch Ball Grid Array (6 x 8 x 1 mm) (Pb-free)	
	CY62126DV30LL-55ZI	51-85087	44-pin TSOP II	Automotive
	CY62126DV30LL-55ZXI		44-pin TSOP II (Pb-free)	
	CY62126DV30L-55BVXE	51-85150	48-ball Fine-Pitch Ball Grid Array (6 x 8 x 1 mm) (Pb-free)	
	CY62126DV30L-55ZSXE	51-85087	44-pin TSOP II (Pb-free)	

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

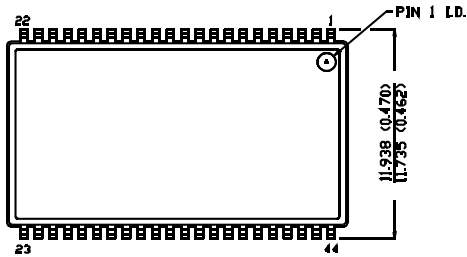
48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



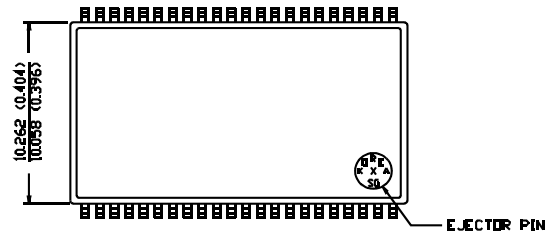
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Package Diagrams(continued)

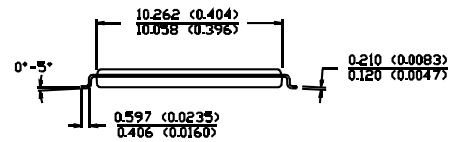
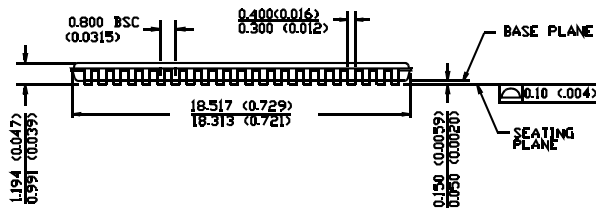
44-pin TSOP II (51-85087)



TOP VIEW



BOTTOM VIEW



51-85087-A

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Document History Page

Document Title: CY62126DV30 MoBL® 1-Mbit (64K x 16) Static RAM Document Number: 38-05230				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117689	08/27/02	JUI	New Data Sheet
*A	127313	06/13/03	MPR	Changed From Advanced Status to Preliminary. Changed I _{SB2} to 5 μA (L), 4 μA (LL) Changed I _{CCDR} to 4 μA (L), 3 μA (LL) Changed C _{IN} from 6 pF to 8 pF
*B	128340	07/22/03	JUI	Changed from Preliminary to Final Add 70-ns speed, updated ordering information
*C	129002	08/29/03	CDY	Changed I _{CC} 1 MHz typ from 0.5 mA to 0.85 mA
*D	238050	See ECN	AJU	Fixed typo: Changed t _{DBE} from 70 ns to 35 ns
*E	316039	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #8 on page #4 Added Pb-free package ordering information on page # 9 Changed 44-pin TSOP-II package name from Z44 to ZS44
*F	335861	See ECN	SYT	Added Temperature Ranges in the Features Section on Page # 1 Added Automotive Product Information for CY62126DV30-L for 55 ns Added I _{SB1} and I _{SB2} values for Automotive range of CY62126DV30-L for 55 ns Added Automotive Information for I _{CCDR} in the Data Retention Characteristics table Added Pb-free packages in the ordering information Changed 44-pin TSOP-II package name from ZS44 to Z44
*G	357256	See ECN	PCI	Added Pin Configuration and Package Diagram for 56-Lead QFN Package Updated Thermal Characteristics and Ordering Information Table Added Automotive Specs for I _{Ix} and I _{Oz} in the DC Electrical Characteristics table on Page# 4
*H	486789	See ECN	VKN	Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court" Removed 45 ns and 70ns Speed bin from Product offering Removed 56-pin QFN package Updated Ordering Information Table

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